The VLSI Interconnect Challenge

Avinoam Kolodny

Electrical Engineering Department
Technion – Israel Institute of Technology

VLSI Challenges

System **complexity**

Performance

Tolerance to **digital noise** and **faults**

More challenges…

The Dominant Challenge is

Power dissipation!

Interconnect

is the crux of the problem

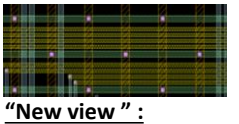
Interconnect

is the crux of the problem

"Old view" of VLSI:

Speed and power are dominated by logic gates

Wires are "ideal"



"New view " :

Logic is fast and virtually free

Speed and power are limited by wires

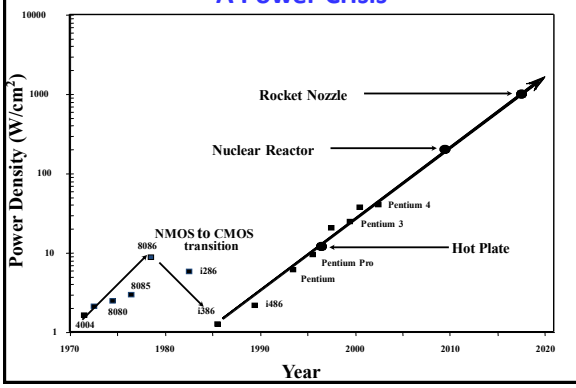
Outline of this talk

Background of the VLSI interconnect challenge

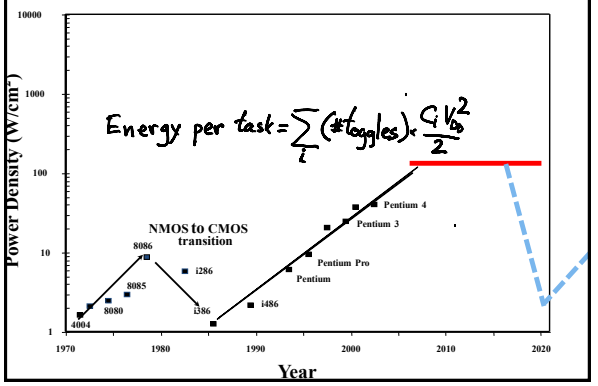
Implications for energy-efficient computing

Research directions

2001 - Extrapolation Towards A Power Crisis



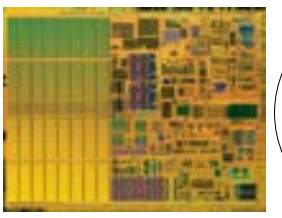
VLSI hits the power wall

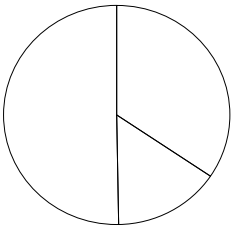


Interconnect Power: A case study - 2004

Intel's Pentium-M, low-power microprocessor, 0.13 micron CMOS

Bit-Transportation energy is larger than computation energy!



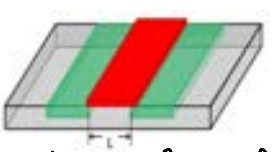


Chips are Like Cities: Complexity is Shown in Connectivity

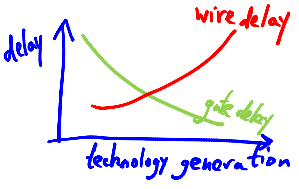
In each generation of technology:

- More transistors
- More interconect wires

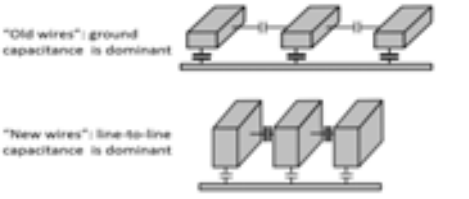
Technology Scaling: Faster Transistors, Slower Wires

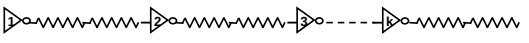


Technology Scaling: Faster Transistors, Slower Wires



Trying to Keep Wire Resistance in Check Leads to Larger Capacitances

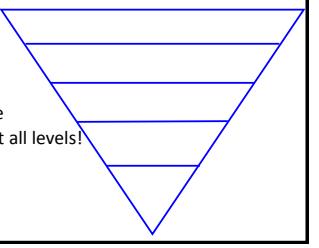




If Bits Were Cars….

$$\text{Energy per task} = \sum_i (\#\text{toggles})_i \cdot \frac{C_i V_{DD}^2}{2}$$

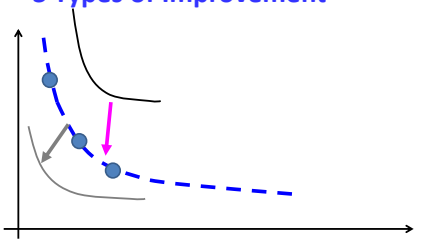
The Nature of Design for Low-Power



No critical root cause

- Because power is cumulative
- Need power-saving efforts at all levels!

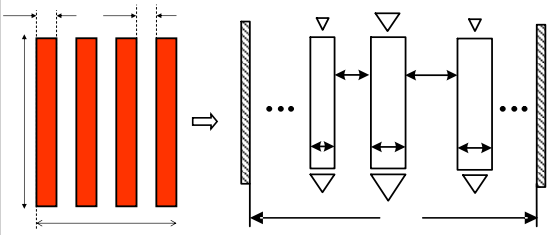
3 Types of Improvement



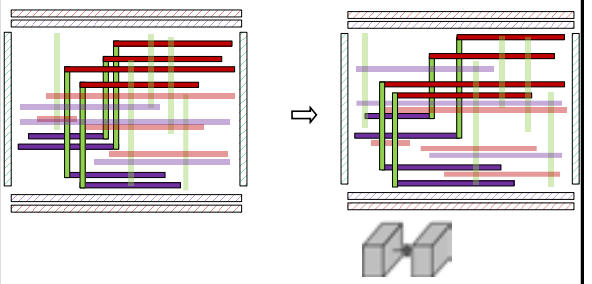
1 Reduce waste of energy
2 (Optimal) Tradeoff power with delay (or other metric)
3 Change the algorithm or computational task

Wire layout optimization:

Wire Widths and Spaces in a Wire Bundle



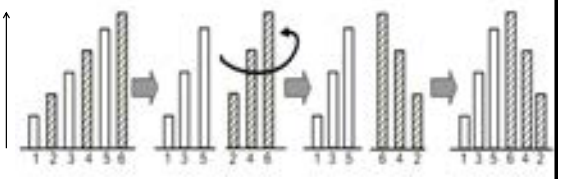
Wire layout optimization:
Finding Optimal Wire Widths and Spaces under Delay Constraints



Integration, 2014.

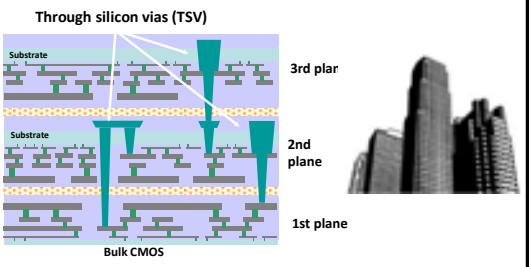
Wire layout optimization:
Optimal Ordering Theorem for Power

Given an interconnect channel with wires of uniform width W, use 'Symmetric Hill' ordering according to activity factors of the signals



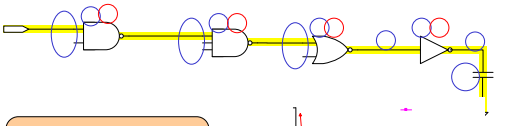
INTEGRATION, 2007

3-D Integrated Circuit Technology



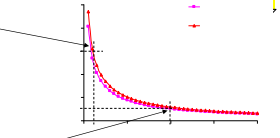
*R. J. Gutmann *et al.*, "Three-Dimensional (3D) ICs: A Technology Platform for Integrated Systems and Opportunities for New Polymeric Adhesives," *Proceedings of the Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173-180, October 2001

Circuit optimization:
Optimal Power-Delay Tradeoff for Logic Paths

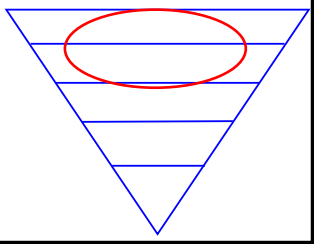


For 2.5% delay increase, get 12x2.5=30% energy reduction!

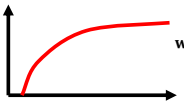
For 20% delay increase, get 2x20=40% energy reduction



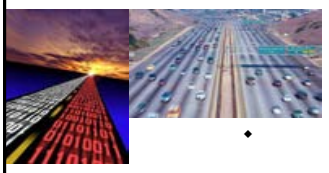
Most Power Savings Can be Made at High Abstraction Levels



Pollack's Rule on Power Efficiency of Uniprocessors

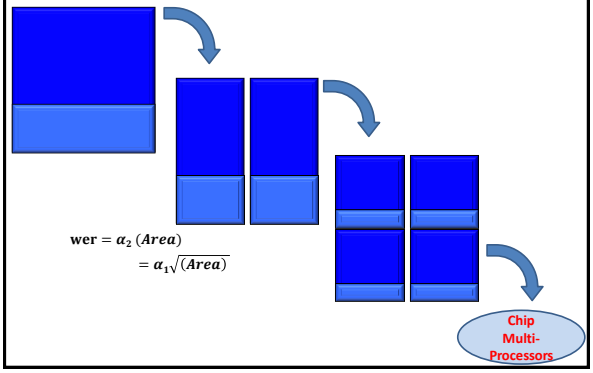


$$\text{wer} = \alpha_2\,(Area)$$
$$= \alpha_1\sqrt{(Area)}$$



Architecture optimization:

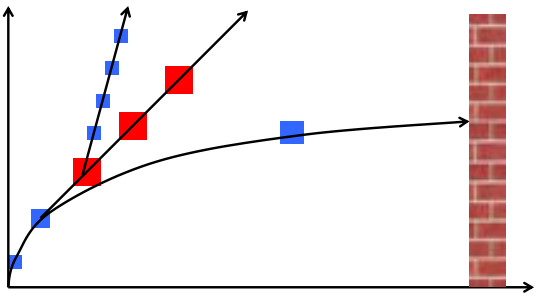
Processor System Evolution to CMP



$$\text{wer} = \alpha_2\,(Area)$$
$$= \alpha_1\sqrt{(Area)}$$

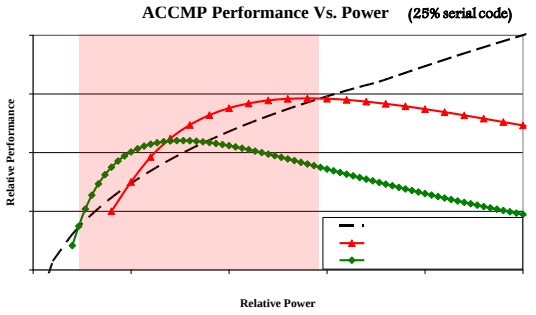
Processor Architectures:

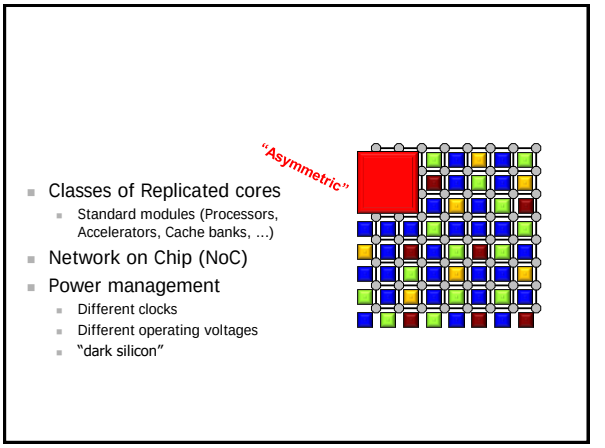
Uni-core, Symmetric multicore, Asymmetric (Heterogeneous)



Architecture optimization:

Asymmetric Multi-Core Performance

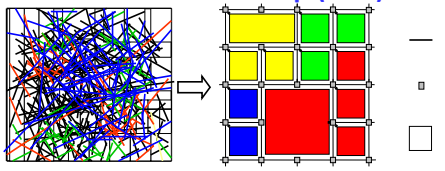




If a chip is like a city, Network-on-Chip (NoC) is like a subway system

Architecture optimization:

Network on-Chip (NoC)



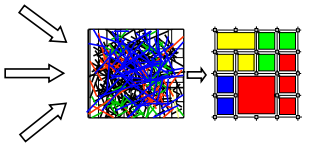
Issues Addressed by NoC

Global wire design

(delay, **power**, noise, scalability, reliability issues)

System integration productivity

(key to modular design)

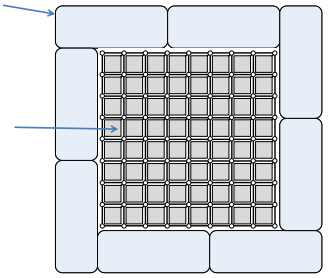


Multi-Core Processor Systems

(key to power-efficient computing)

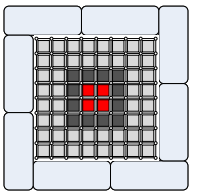
Interconnect-aware and NoC-aware Architectural Research

Accessing On-Chip Cache Banks through a NoC



Where to Store the Shared Data?

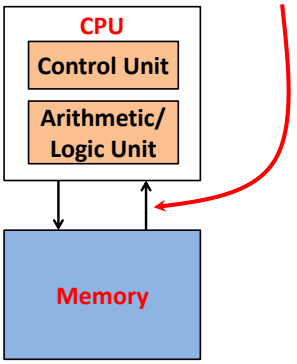
A small number of lines, shared by many processors, is accessed numerous times



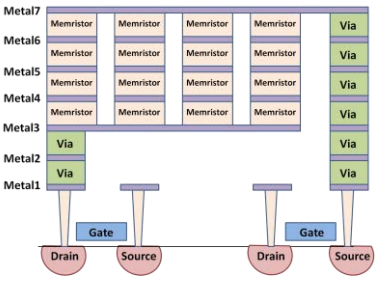
What can be done better?

- Bring shared data closer to all processors
- Preserve vicinity of private data

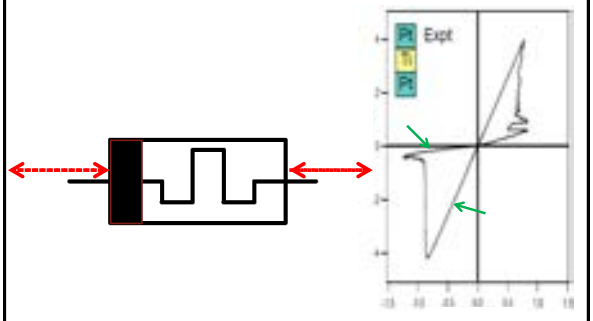
Memory Bottleneck



Reducing Distances by Embedding Memory in Execution Units

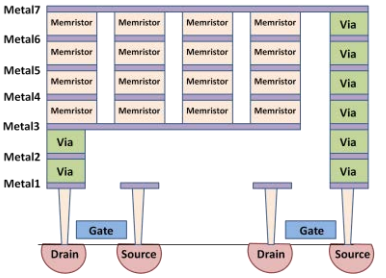


Memristor Devices

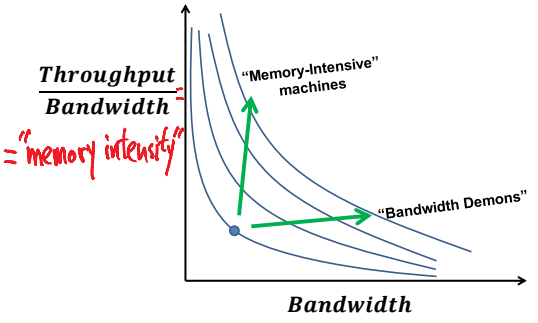


Sea of Memory

Dense and fast



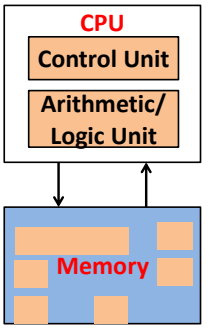
Towards Memory-Intensive Machines



Constant-throughput-curves
➔ increase on-die-memory!

Logic within the Memory

Beyond von Neumann Architecture



Summary

VLSI power is dominated by interconnect!

New architectures are driven by interconnect distances/latencies/power