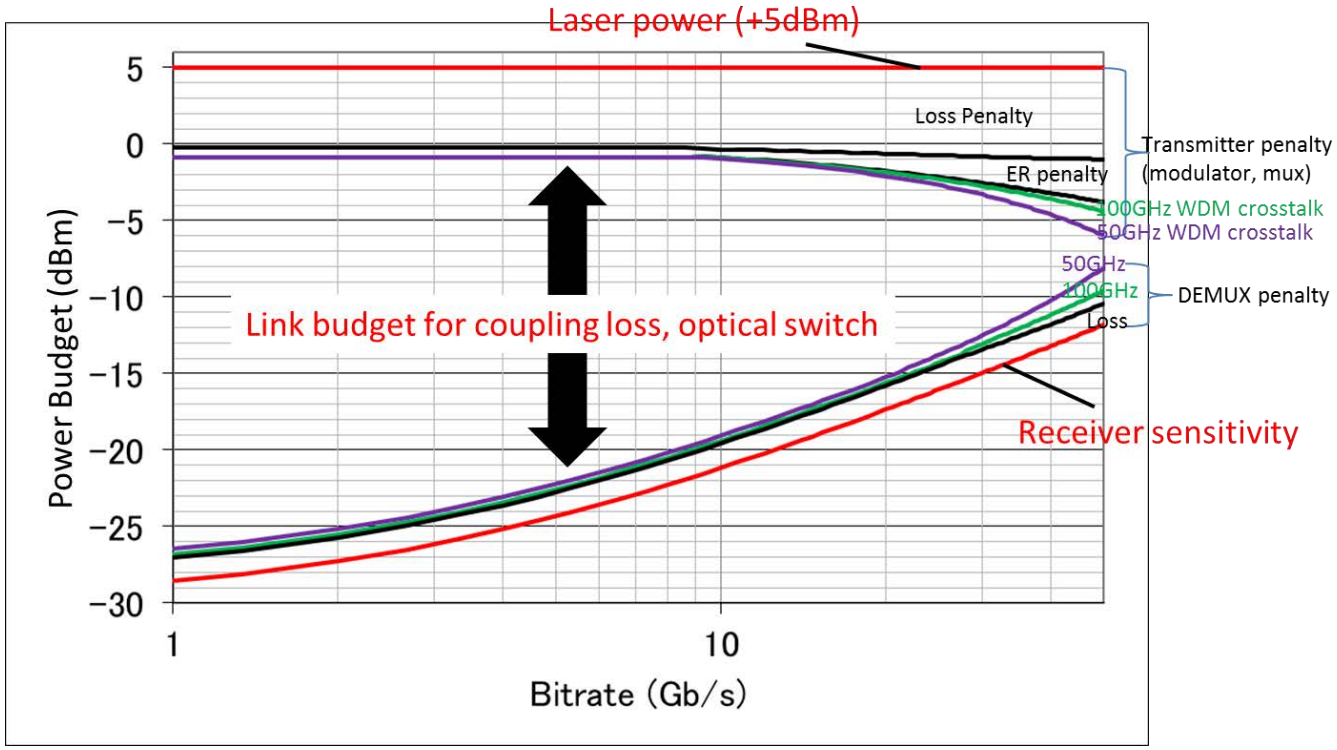
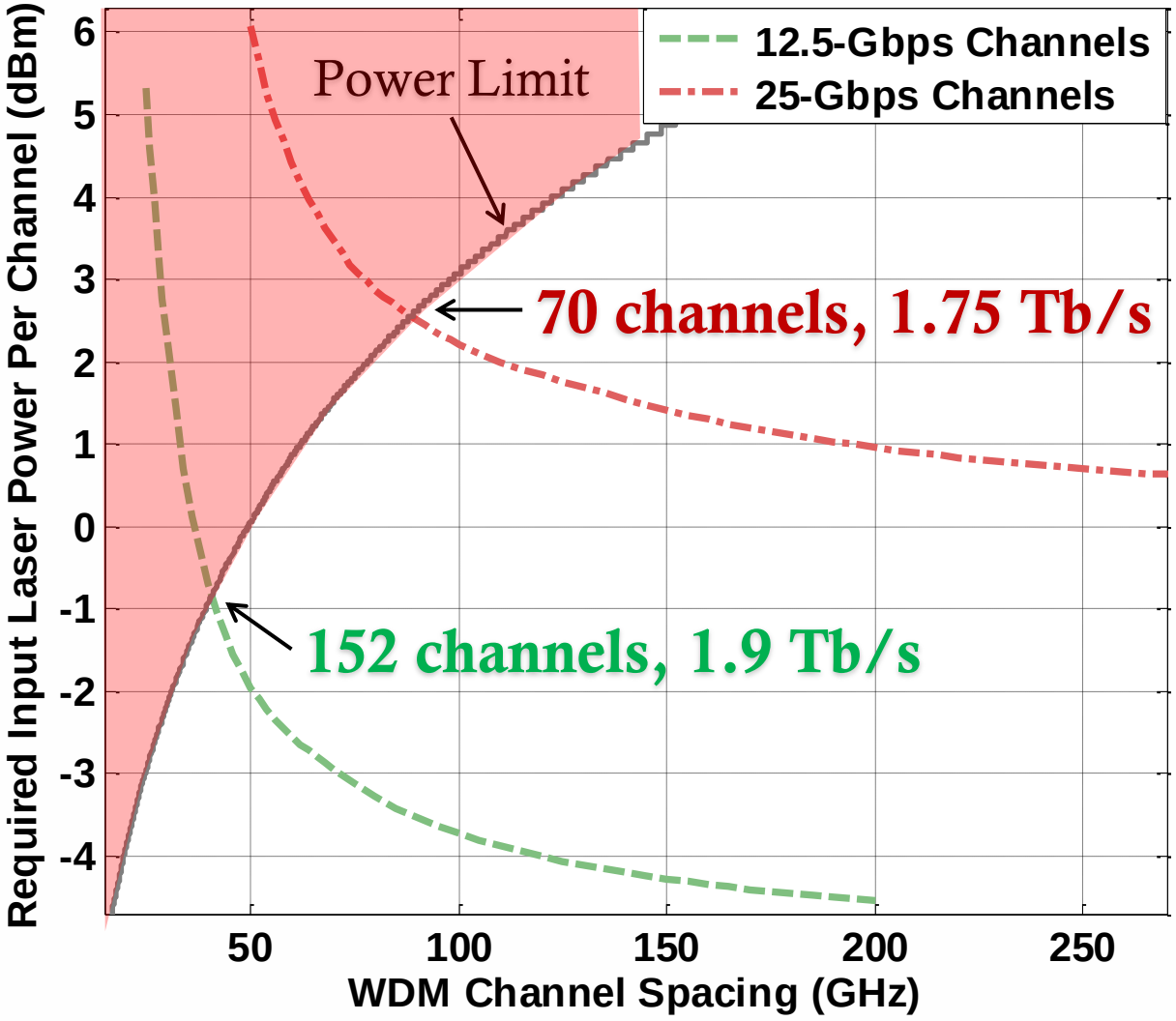

Laser power (+5dBm)
Loss Penalty
Transmitter penalty
(modulator, mux)
ER penalty
100GHz WDM crosstalk
50GHz WDM crosstalk
50GHz
100GHz
DEMUX penalty
Loss
Link budget for coupling loss, optical switch
Receiver sensitivity
Power Budget (dBm)
5
0
−5
−10
−15
−20
−25
−30
1
10
Bitrate (Gb/s)

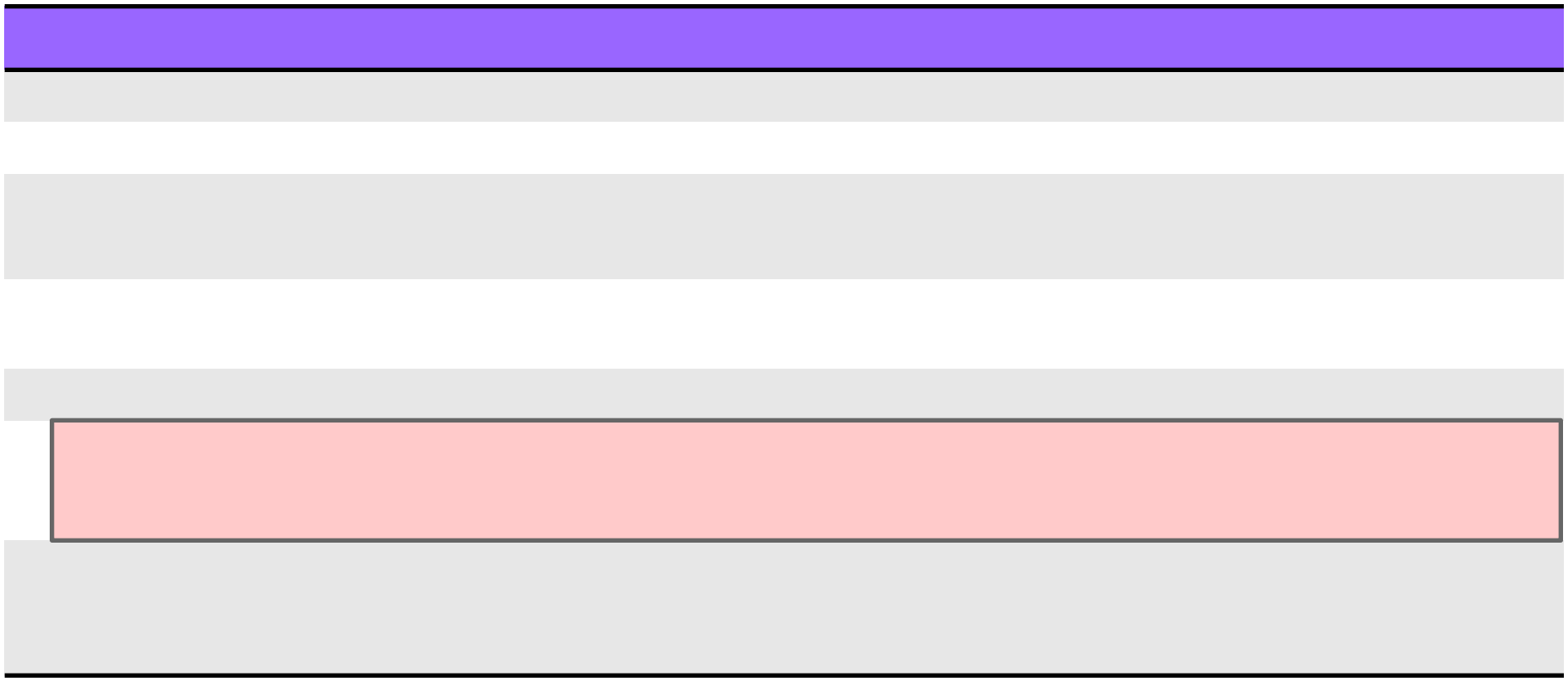
Optical Power Budget



Power per channel inversely proportional to channel spacing.

20-dBm power limit determines achievable BW.

12.5 Gb/s test case more scalable. Mainly because of receiver sensitivity.



2.3 pJ/b

4.1 pJ/b

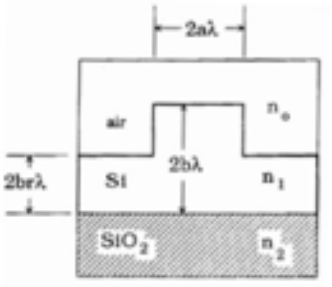
Path to Commercialization: Silicon Photonic Technology

Fundamental Discoveries

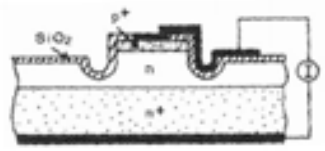
Introduction of Innovative Devices and Processes

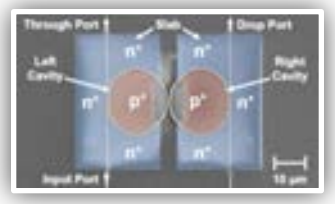
Integration and Commercialization

- low-loss, single-mode waveguiding

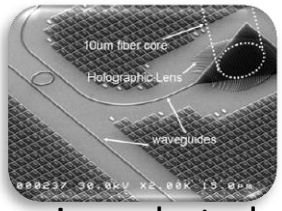


- optical coupling
- optical modulation via carrier injection

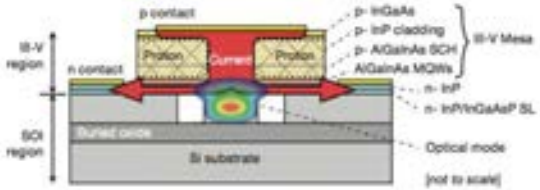




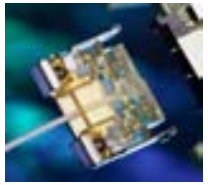
- high-speed microring modulators and switches
- arrayed waveguide gratings



- Germanium photodetectors
- ultra low-loss waveguides and crossings
- hybrid silicon lasers



Hybrid platforms



intel

Monolithic CMOS Integration

IBM

ORACLE

Transceivers for Datacom

APIC CORPORATION

LUXTERA NANOPHOTONIC INTEGRATED CIRCUITS

Foundry Services

Institute of Microelectronics A*STAR

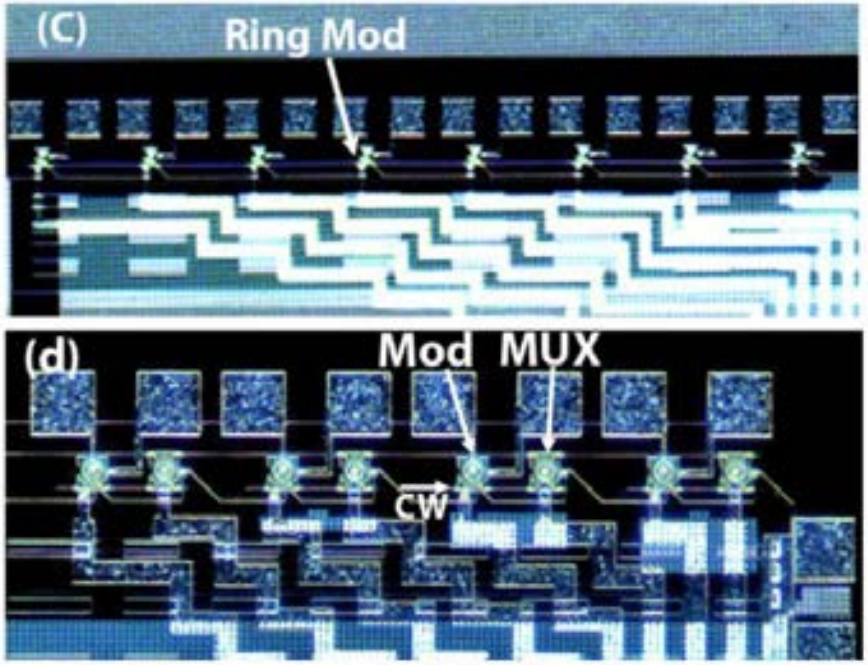
OpSIS

imec

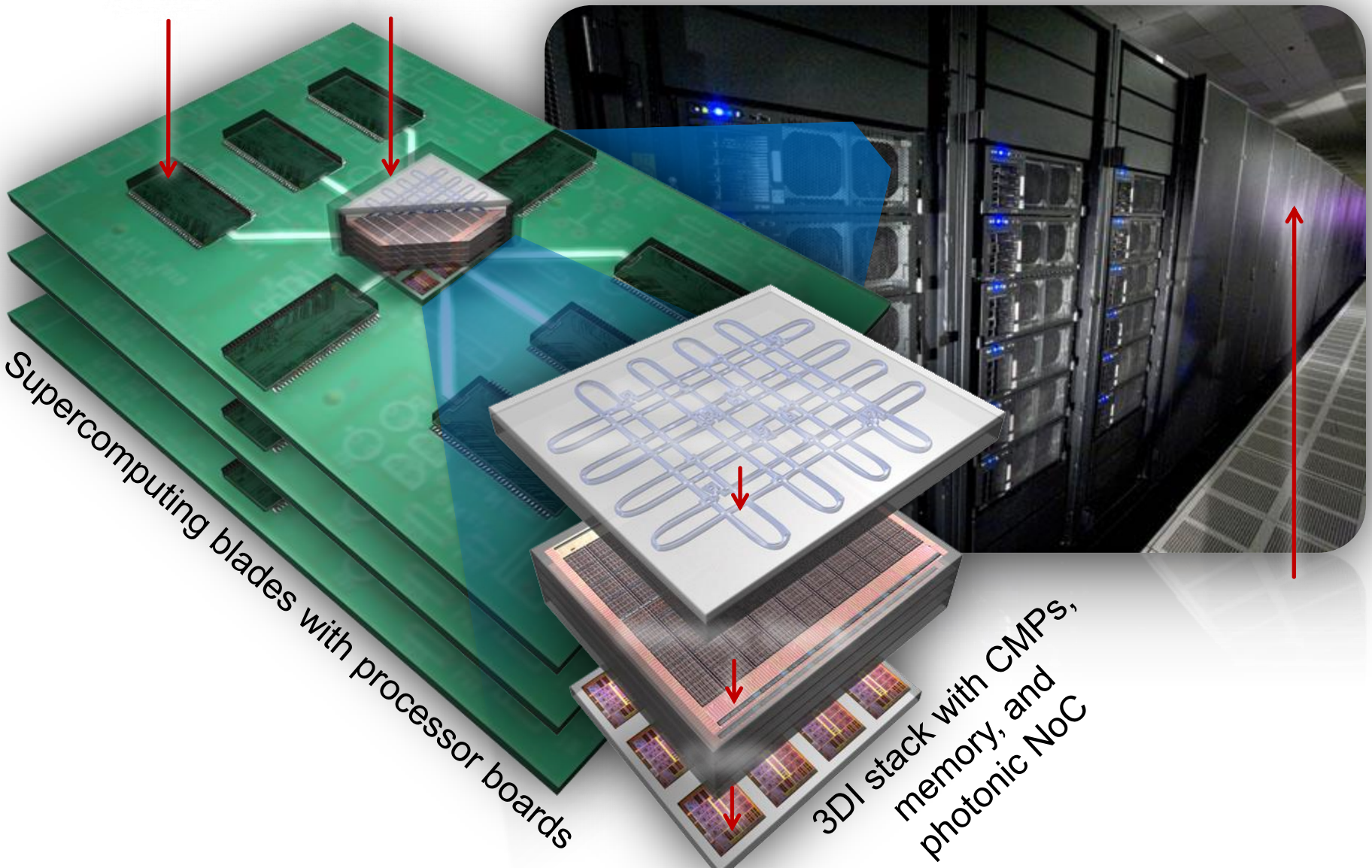
1990s 2000s 2010 2013 +

320 Gb/s WDM transmitters based on silicon microrings

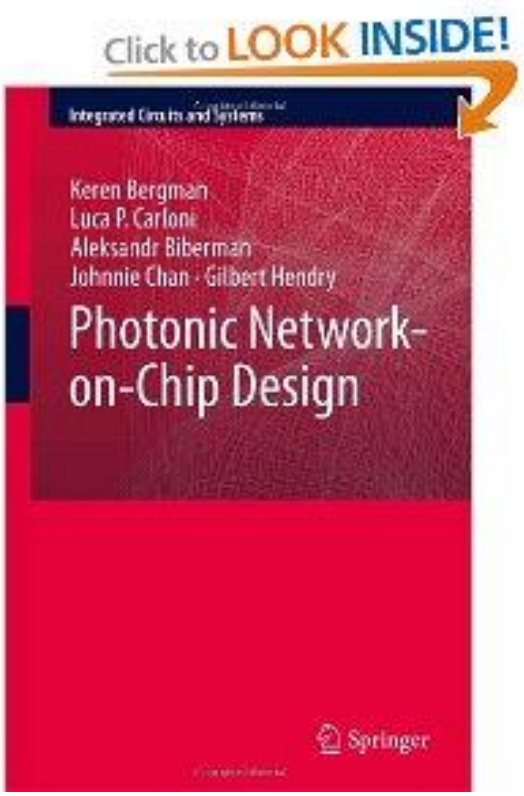
- 8-channel WDM transmitter based on conventional common-bus architecture
- 32fJ/bit modulation power efficiency, less than 0.04 chip area
- highest aggregated data rate achieved in silicon transmitters



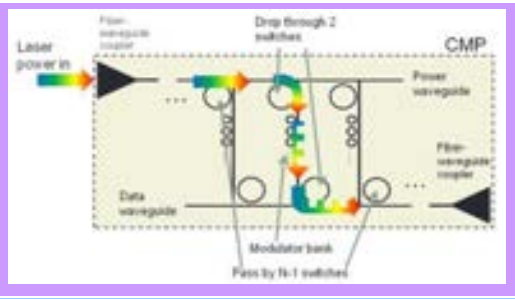
Silicon Photonics for Exascale Computing

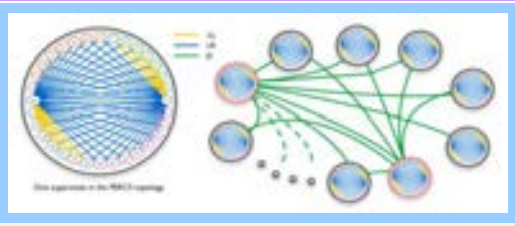


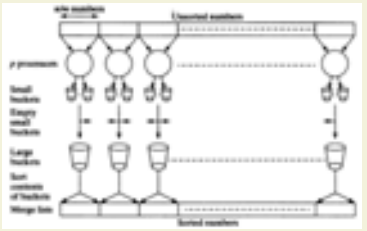
Photonic Network-on-Chip Design

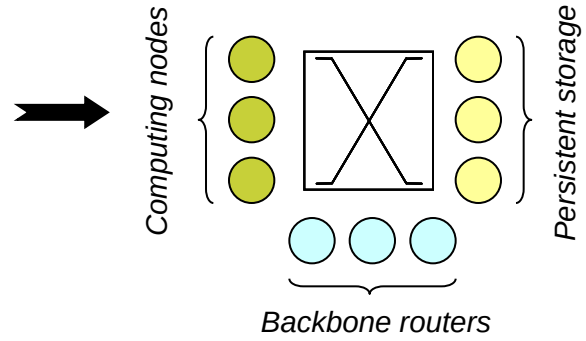


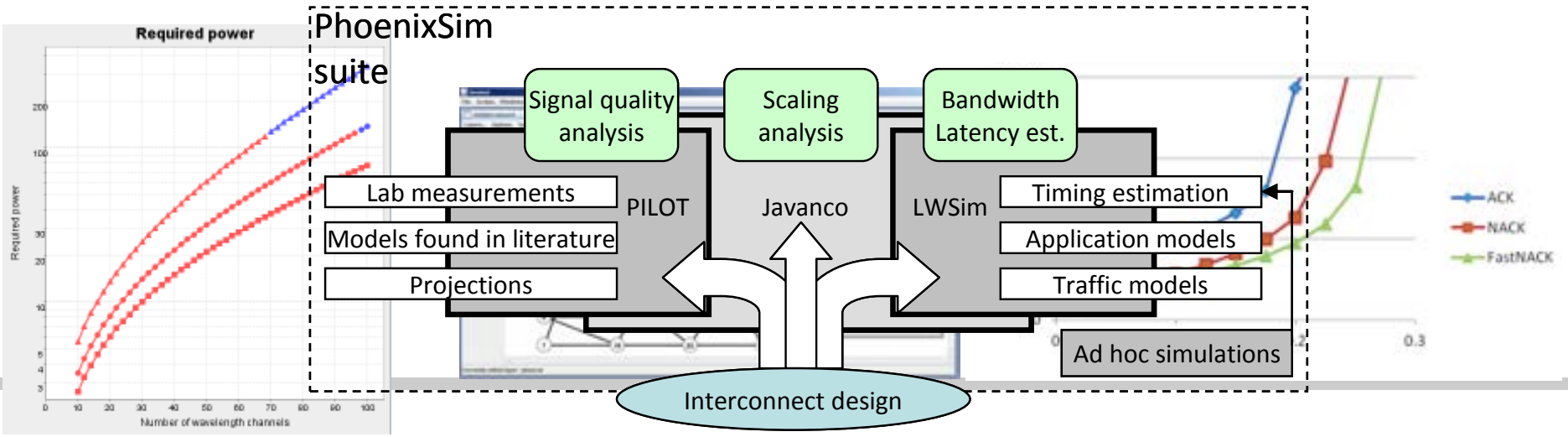
Photonic-Enabled Systems: Multi-Level Co-Design

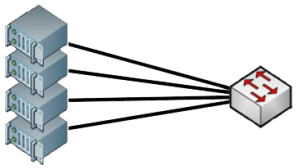


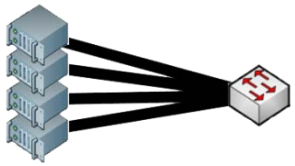


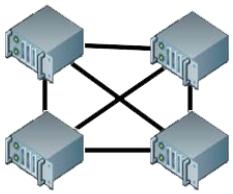


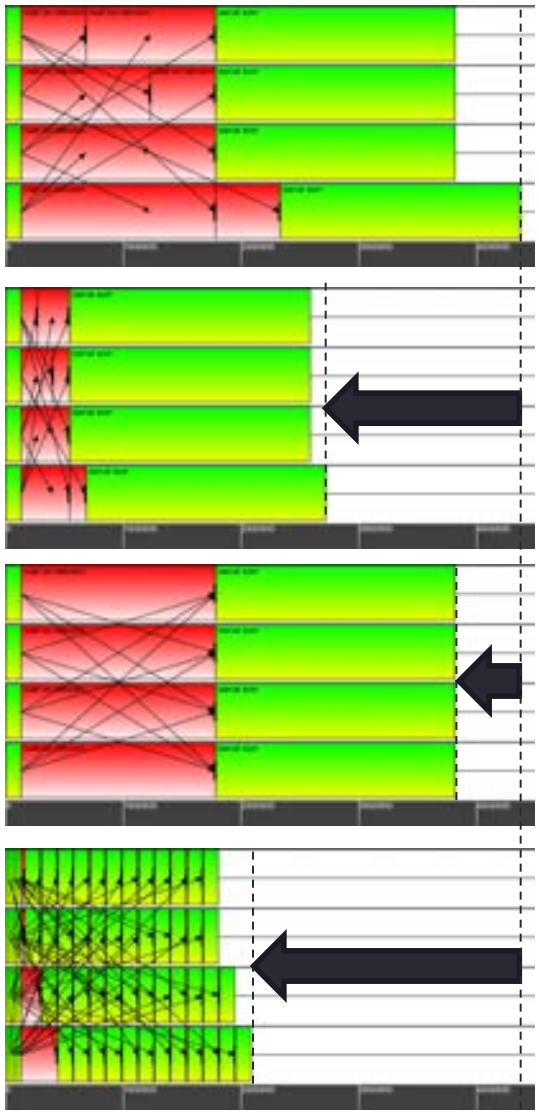

Computing nodes
Persistent storage
Backbone routers

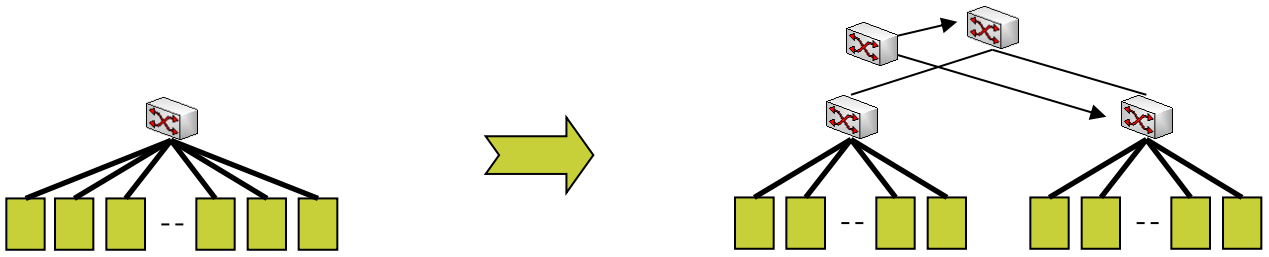

Required power
Required power
Number of wavelength channels
PhoenixSim suite
Signal quality analysis
Scaling analysis
Bandwidth Latency est.
Lab measurements
Models found in literature
Projections
PILOT
Javanco
LWSim
Timing estimation
Application models
Traffic models
Ad hoc simulations
Interconnect design
ACK
NACK
FastNACK

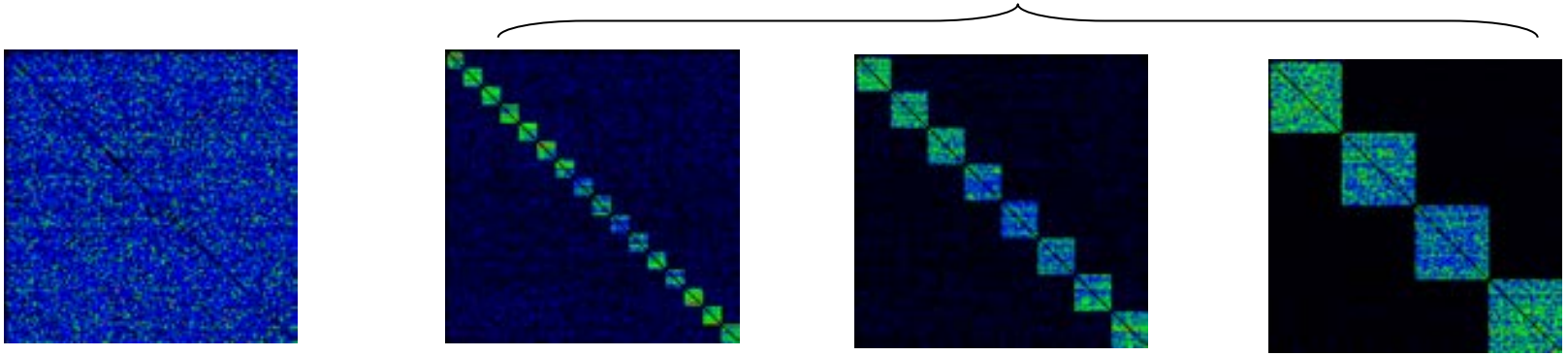


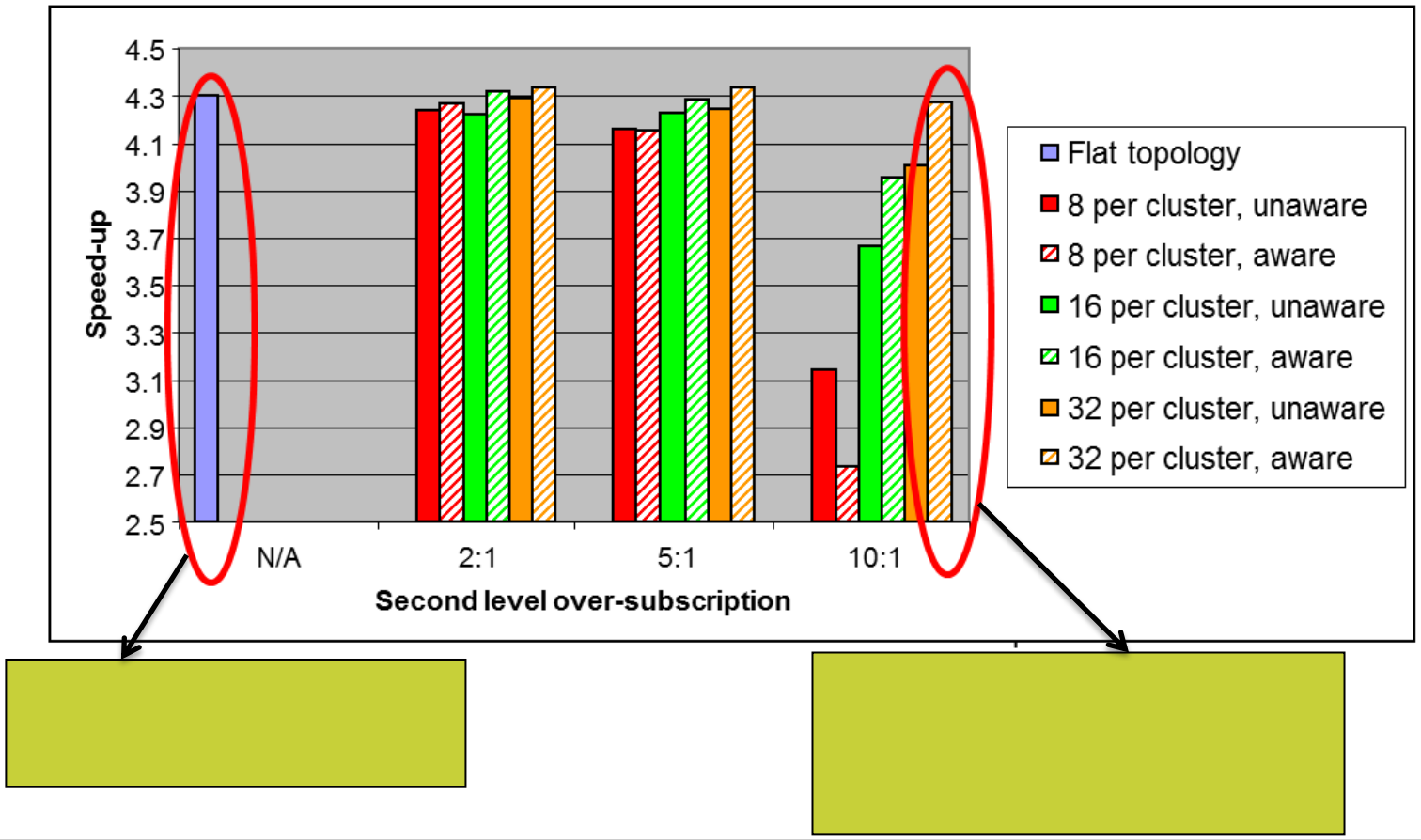






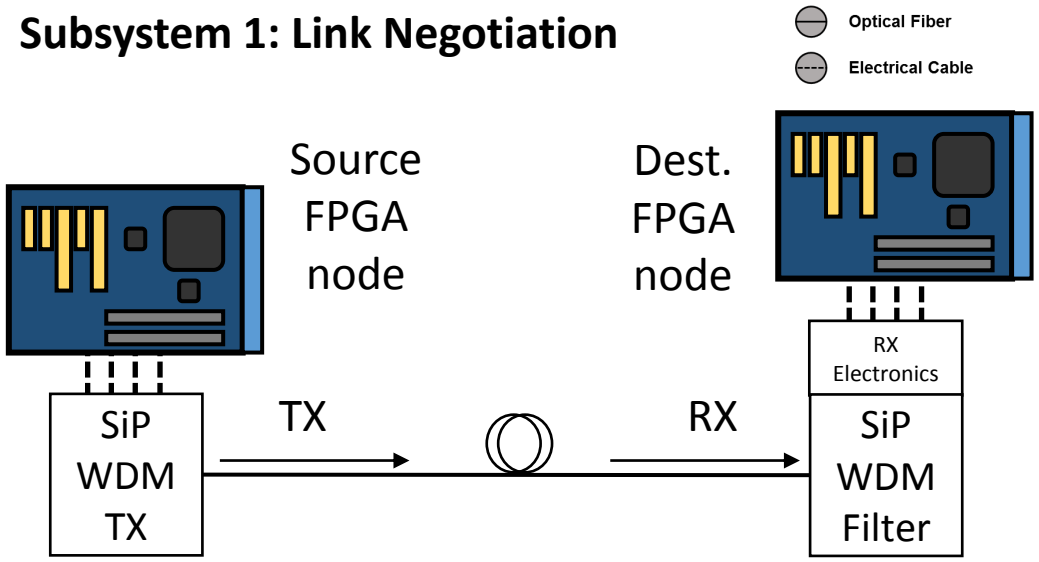


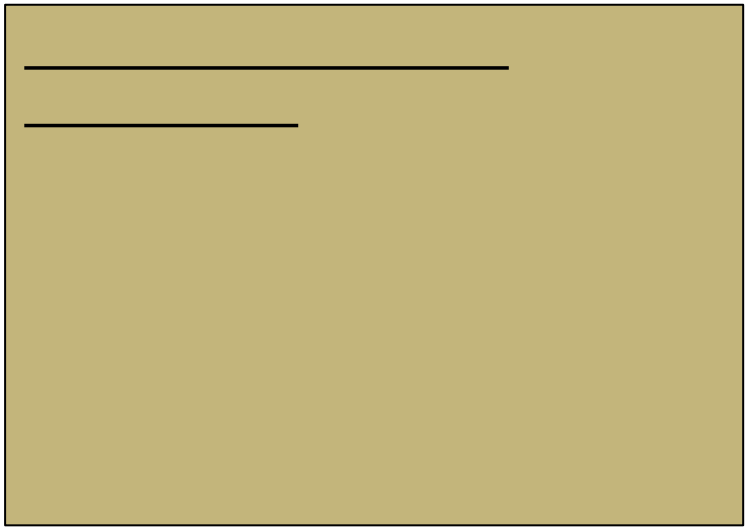


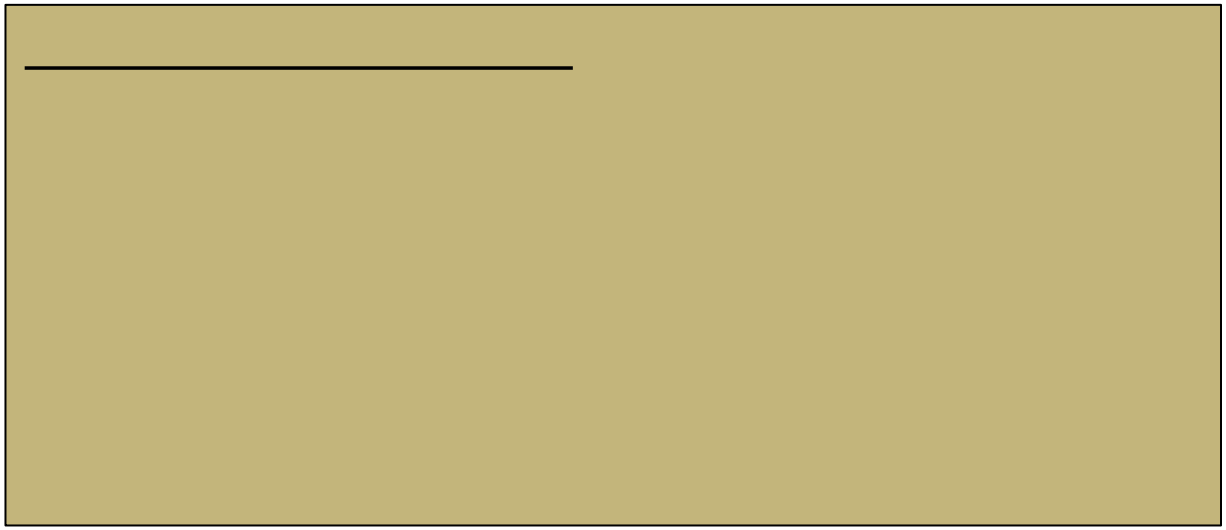

4.5
4.3
4.1
3.9
3.7
3.5
3.3
3.1
2.9
2.7
2.5
Speed-up
N/A
2:1
5:1
10:1
Second level over-subscription
Flat topology
8 per cluster, unaware
8 per cluster, aware
16 per cluster, unaware
16 per cluster, aware
32 per cluster, unaware
32 per cluster, aware

FPGA-Controlled Silicon Photonic Interconnected System
Optical Network Interface: O-NIC Link Negotiation and Control

Subsystem 1: Link Negotiation



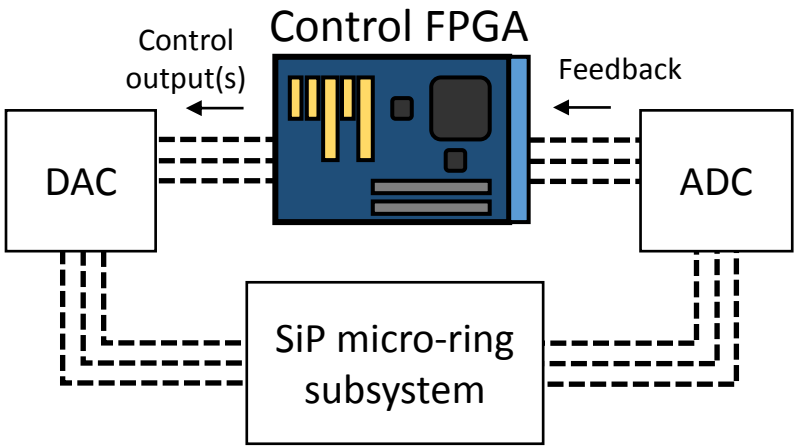




FPGA-Controlled Silicon Photonic Interconnected System

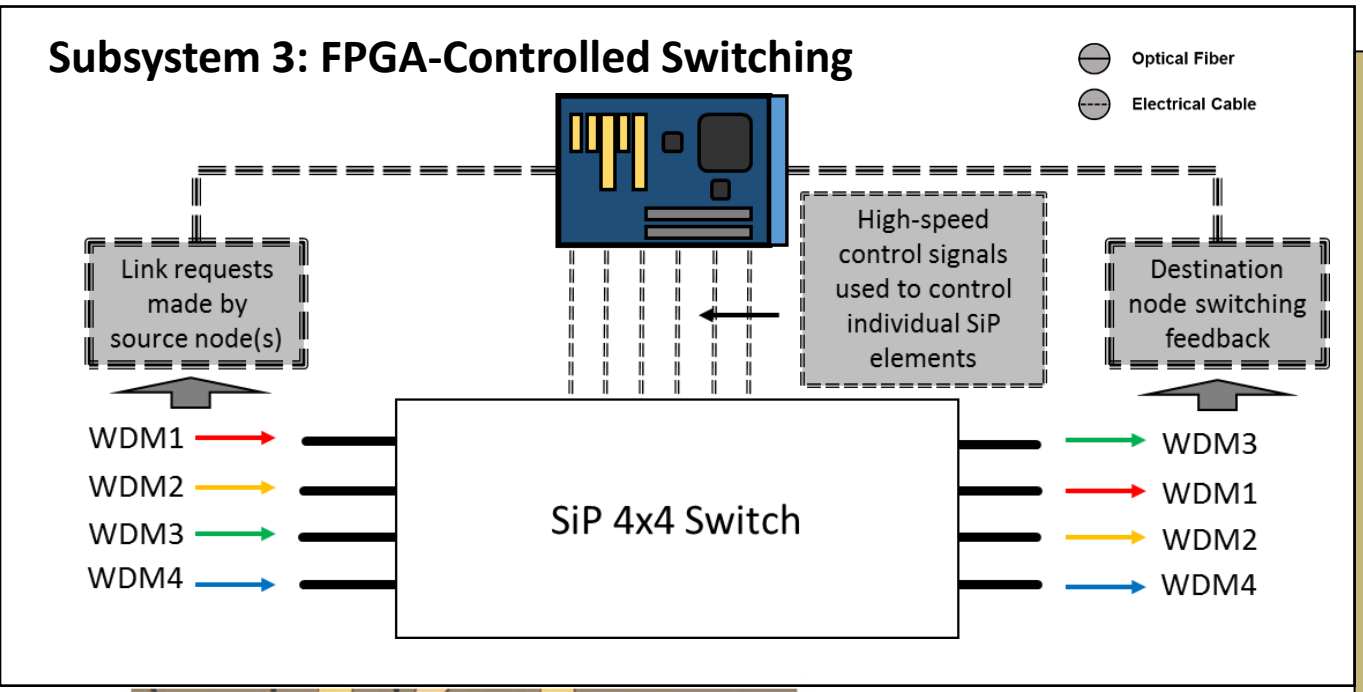
Subsystem Thermal Control and Operation

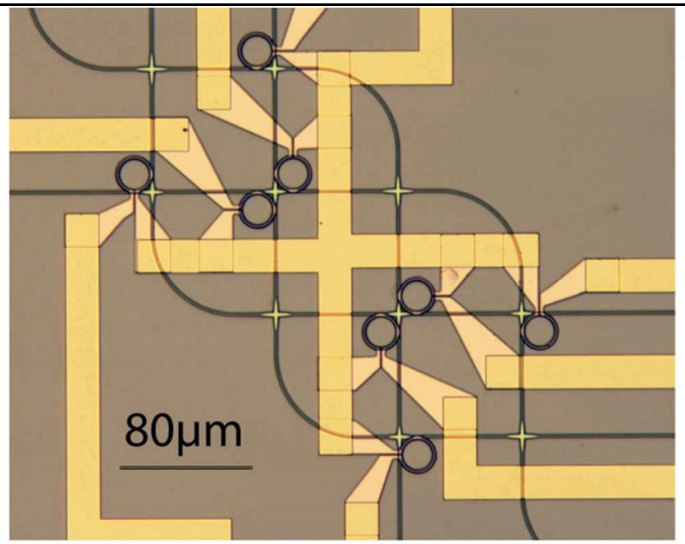
Subsystem 2: SiP Device Control



FPGA-Controlled Silicon Photonic Interconnected System

Switch Fabric Control and Arbitration



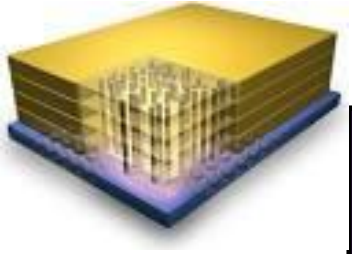


[N. Sherwood-Droz *et. al.*, *Optics Express,* 2008]

4x4 Microring Switch Routing Table

State Number	I/O Combination				
	N	S	E	W	Rings Used
1	W	N	S	E	R2,R3,R8,R5
2	W	E	N	S	R2,R7
3	W	E	S	N	R2,R7,R8,R1
4	S	N	W	E	R6,R3,R4,R5
5	S	W	N	E	R6,R5
6	S	E	W	N	R6,R7,R4,R1
7	E	W	S	N	R8,R1
8	E	W	N	S	none
9	E	N	W	S	R1,R4

Silicon Photonic Interconnected Micron Hybrid Memory Cube



HMC
(2GB, gen2)

Stratix 10 FPGAs –
(Tentative release date 2015)

1.28 Tbps bisectional bandwidth

8 bidir. lanes @ 40 Gbps per FPGA

FPGA (Stratix 10)

FPGA (Stratix 10)

FPGA (Stratix 10)

FPGA (Stratix 10)

SiPh WDM Tx/Rx chip

SiPh WDM Tx/Rx chip

SiPh WDM Tx/Rx chip

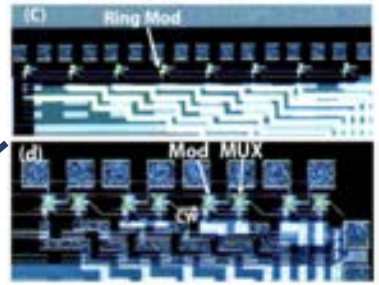
SiPh WDM Tx/Rx chip

320 Gbps Tx 320 Gbps Rx

320 Gbps Tx 320 Gbps Rx

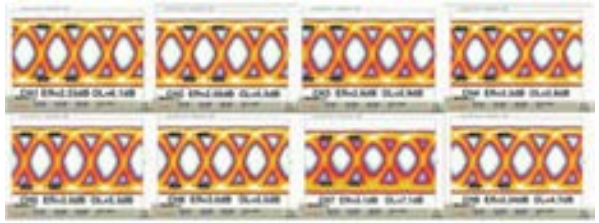
320 Gbps Tx 320 Gbps Rx

320 Gbps Tx 320 Gbps Rx



8 WDM CH SiPh Chip (OPSIS)

8 X 40Gb/s eye diagrams



6x6 SiPh MZI-based switch

640 Gbps Tx 640 Gbps Rx

Board I/O

1.28 Tbps bisectional bandwidth

Scalability of an FPGA-Controlled Silicon Photonic Interconnected System