Vertical-cavity surface-emitting lasers (VCSELs) for “green” optical interconnects

James A. Lott

Dejan Arsenijević, Gunter Larisch, Hui Li, Philip Moser, Philip Wolf

Dieter Bimberg

Institut für Festkörperphysik und
Zentrum für Nanophotonik,
Technische Universität Berlin
Federal Republic of Germany

Halbleiter-Nanophotonik SFB 787

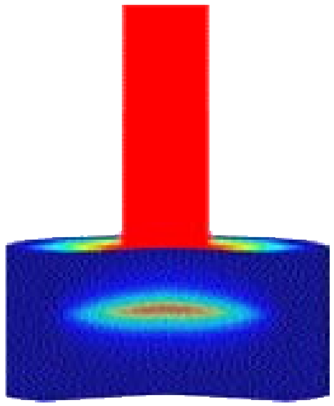
Outline

- **Opportunities in optical interconnects:**
  1) free-space
  2) “medium-reach“ (SR) up to 2 km
  3) “short-reach“ (SR) up to ~300 m
  4) “very-short-reach“ (VSR) < 2 m
  5) “ultra-short-reach“ (USR) < 20 mm

- **VCSELs that are:**
  1) **energy efficient**
  2) capable of high bit rates
  3) highly temperature stable
  4) integrated on-chip

- **Our record VCSEL results**

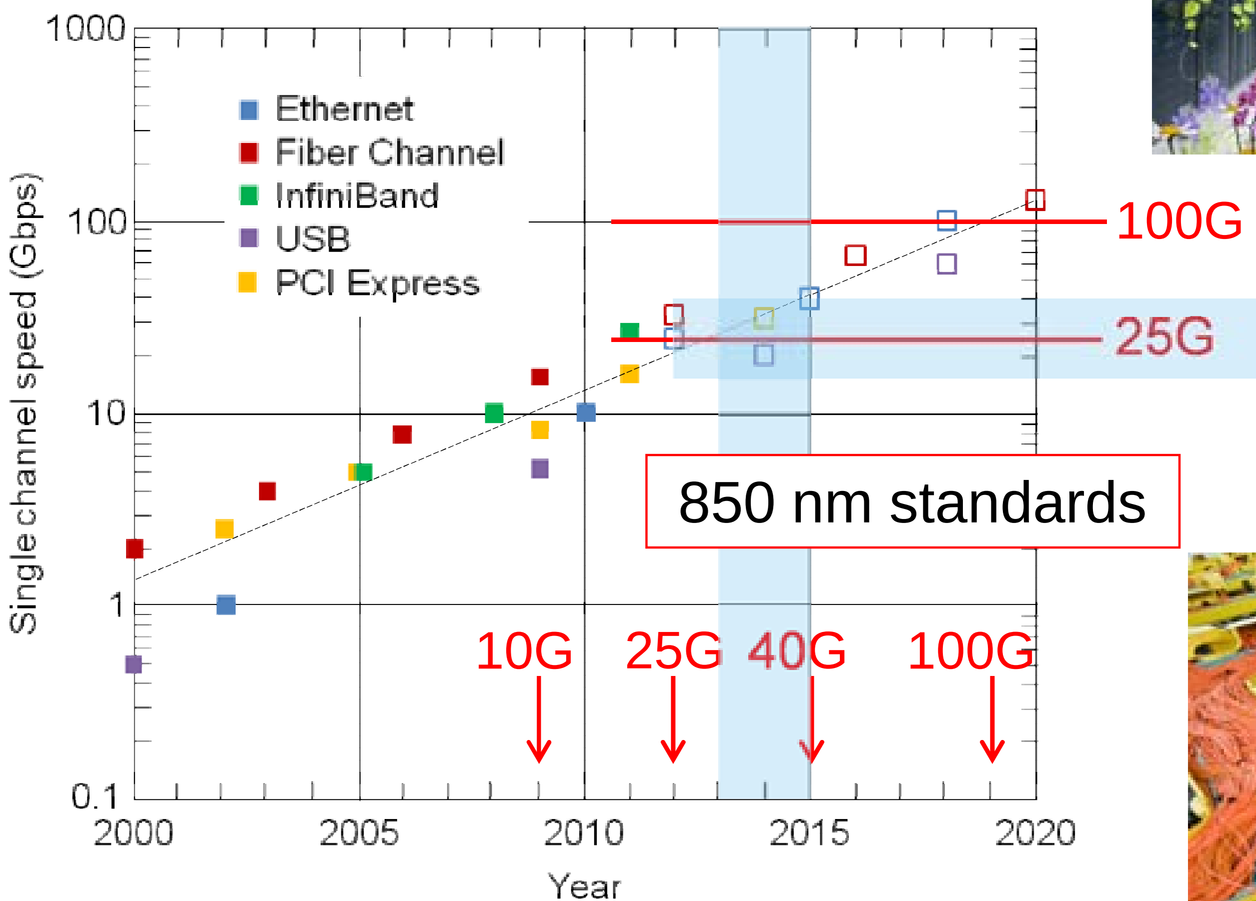
- **Conclusion and outlook**



Optical interconnect **opportunities**

short-reach (SR) optical interconnects: up to ~300 m

want more bandwidth for less energy



A. Larsson *et al.*, *IEEE JSTQE*,17(6) pp.1552-1567 (Nov/Dec 2011).

http://www.42u.com

datacom

http://www.wifinotes.com

energy-efficient VCSELs

a Key Enabling Technology:

SuperMUC, Leibniz-Rechenzentrum, Garching, Germany (3 petaflop/s)

computercom

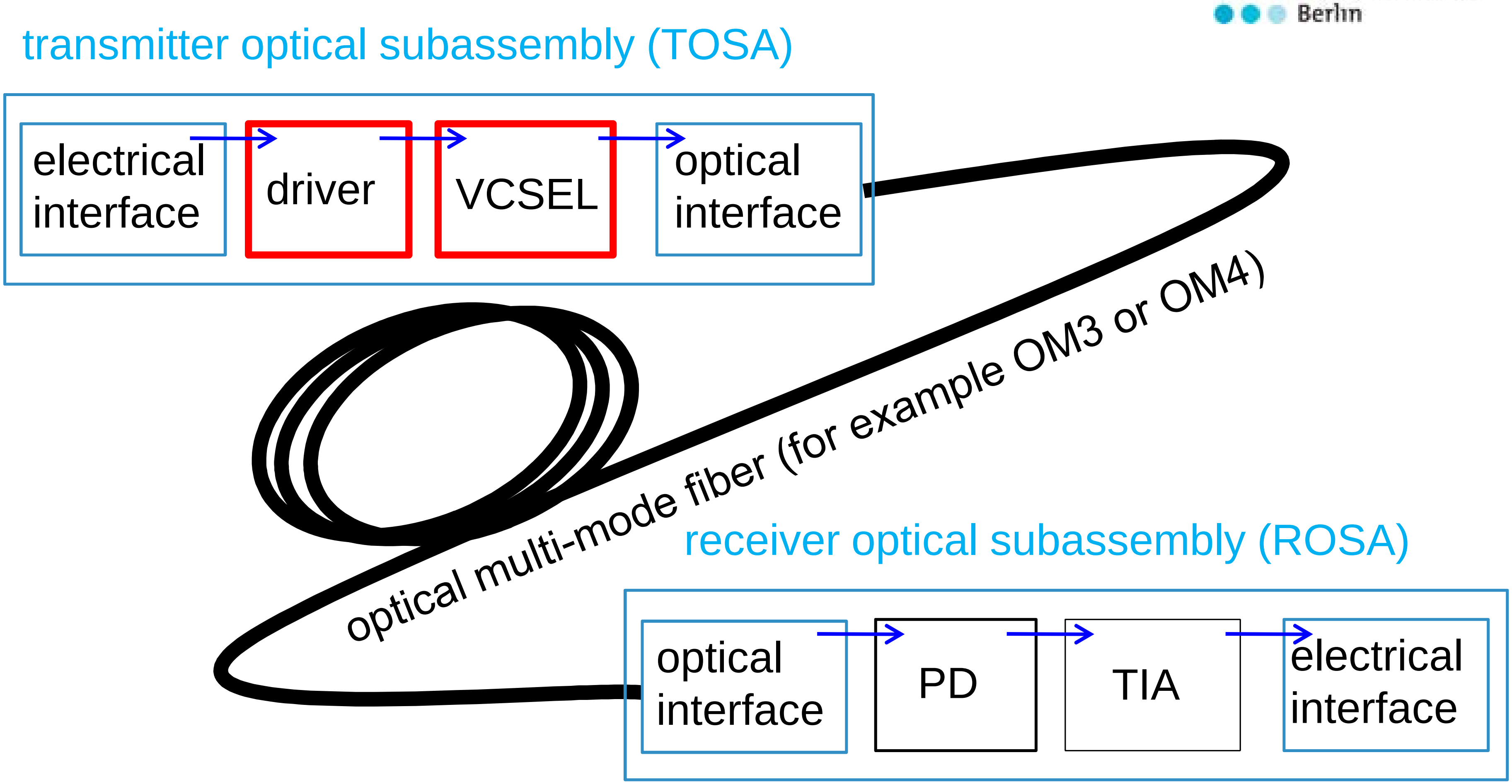
http://www.lrz.de/english/

http://www.gizmodo.com.au/2012/09/25-supercomputers-that-fill-entire-rooms/

VCSEL-based optical link

HiTrans

Investitionsbank Berlin



Programm zur Förderung von Forschung, Innovationen und Technologien (***ProFIT***)

HiTrans: Fundamentals of high bit-rate transceivers for optical interconnect applications

Energy efficiency

Energy-to-data ratio (*EDR*):

$$EDR = \frac{I \cdot V}{BR}$$

in fJ/bit

I: drive current
V: voltage
BR: bit rate

total energy per transmitted bit for (only) the VCSEL

Modulation Energy:

True rms power absorbed in the device.

in fJ/bit

Heat-to-bit rate ratio (*HBR*):*)

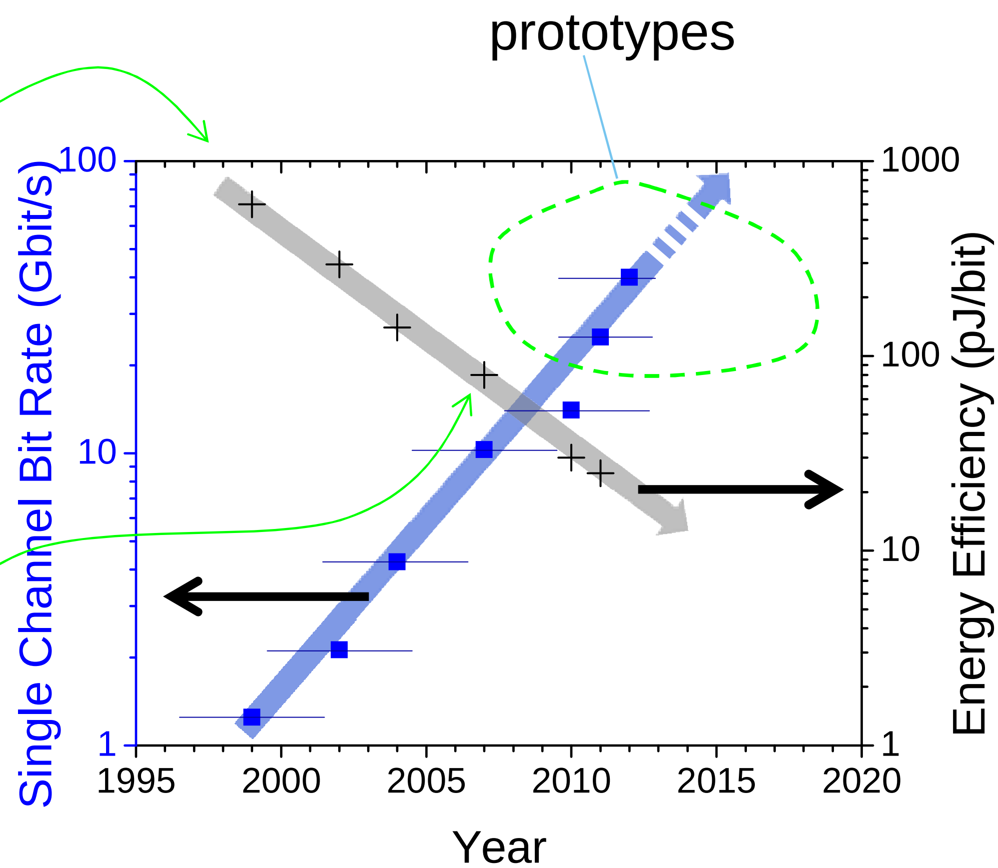
$$HBR = \frac{I \cdot V - P_{opt}}{BR}$$

in mW/Tbps (or fJ/bit)

P_{opt}: optical output power

*) Commonly used in literature

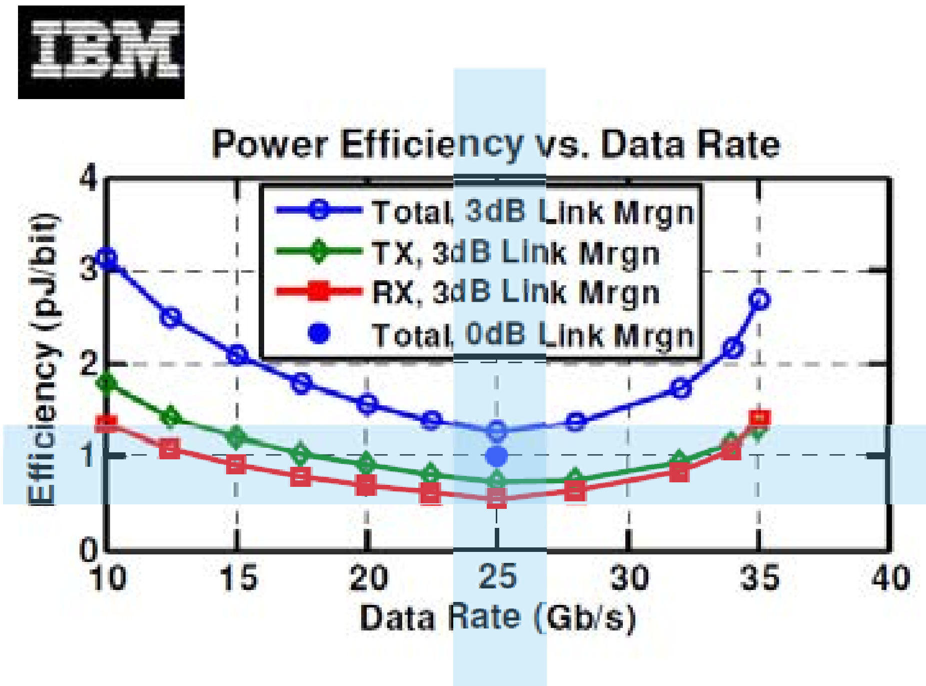
$$\frac{(5\ \text{V})\cdot(150\ \text{mA})}{(1.25\ \text{Gbit/s})} \approx 600\ \text{pJ/bit}$$

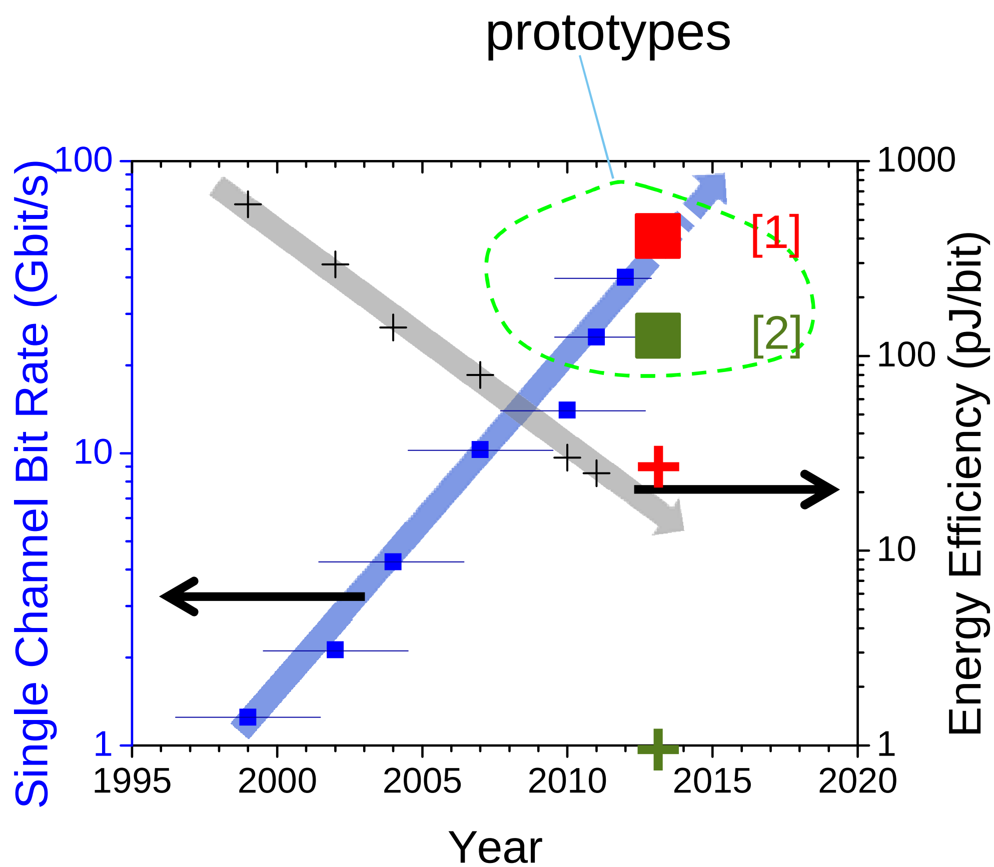


$$\frac{(3.3\ \text{V})\cdot(250\ \text{mA})}{(10.3124\ \text{Gbit/s})} \approx 80\ \text{pJ/bit}$$

- The single channel bit rate is increasing toward ≥ 40 Gbit/s
- The TOSA energy dissipation is decreasing toward ~1 pJ/bit by circa 2020

Focus on “energy efficiency”





- [1] **56.1 Gbit/s** at ~**23.7 pJ/bit**: fast, opportunity to reduce energy/bit
- [2] **25 Gb/s** at ~**1 pJ/bit**: energy-efficient, opportunity to increase bit rate

➡ Need a strategy to increase both bit rate and energy efficiency

[1] Kuchta *et.al.*, IBM & Finisar, OFC 2013, paper OW1B.5
[2] Proesel *et.al.*, IBM & Emcore, OFC 2013, paper OM2H

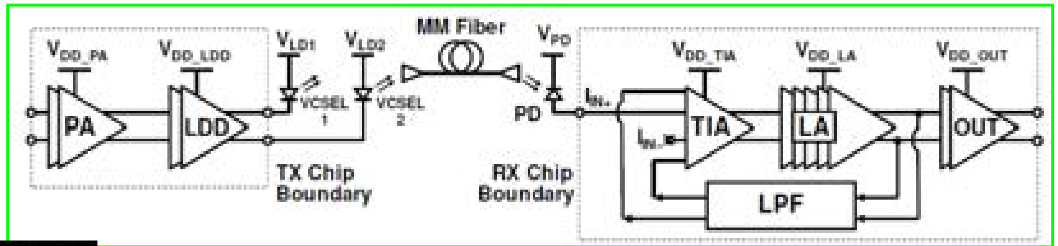
Only ~1 pJ/bit per optical link

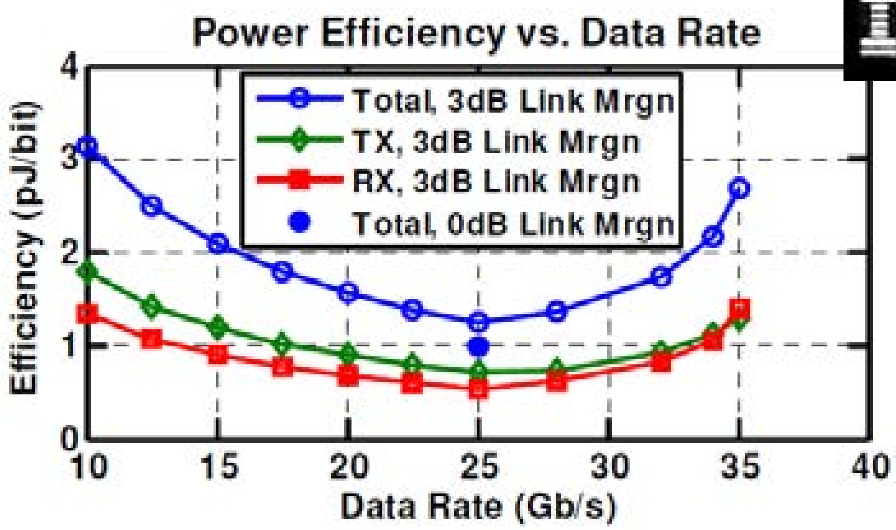
OM2H.2.pdf OFC/NFOEC Technical Digest © 2013 OSA

35-Gb/s VCSEL-Based Optical Link using 32-nm SOI CMOS Circuits

Jonathan E. Proesel, Benjamin G. Lee, Christian W. Baks, and Clint L. Schow
IBM T. J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY 10598
jonproesel@us.ibm.com

4 m OM2 MMF





low power:	25 Gb/s @ 1.0 pJ/bit
nominal power:	28 Gb/s @ 2.0 pJ/bit
high speed:	35 Gb/s @ 2.7 pJ/bit

low power: VCSEL consumes **~41%**
nominal power: VCSEL consumes **~32%**
high-speed: VCSEL consumes **~29.5%**

[2]

56.1 Gbit/s at ~**23.7 pJ/bit;** with SiGe biCMOS the VCSEL energy is ~1-2% of the total link energy (OFC13, 14)

[1]

25 Gb/s at ~**1.0-to-2.7 pJ/bit:** with SOI CMOS the VCSEL energy is ~30-41% of the total link energy

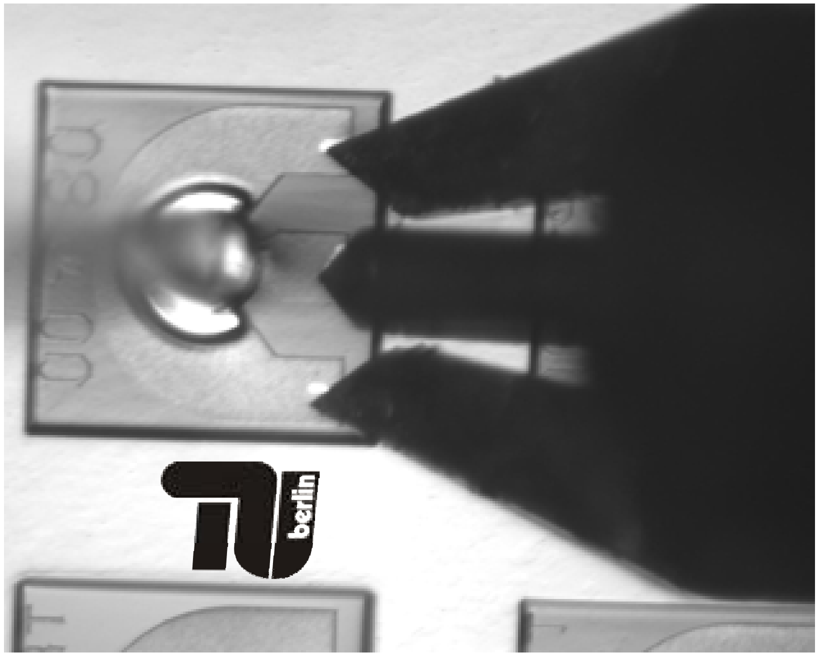
[1] Kuchta *et.al.*, IBM & Finisar, OFC 2013, paper OW1B.5
[2] Proesel *et.al.*, IBM & Emcore, OFC 2013, paper OM2H

VCSELs: a key enabling technology

- want very small energy per bit:
  then the driver needs to provide less power

- low noise of VCSEL emission enables
  the use of simpler PD+TIA configurations

- temperature stability enables simpler and
  less energy consuming driver circuits



an on-chip measurement with a high-frequency GSG microprobe

➡ energy efficient, temperature stable VCSELs enable **an energy efficient** optical interconnect

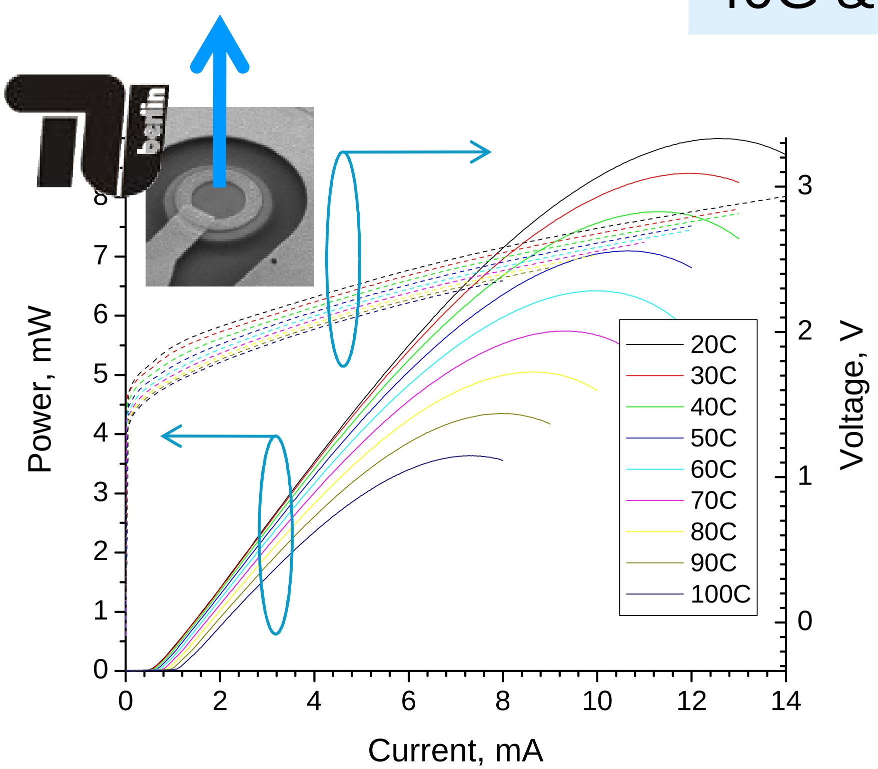
40 Gbit/s 850 nm multimode VCSELs

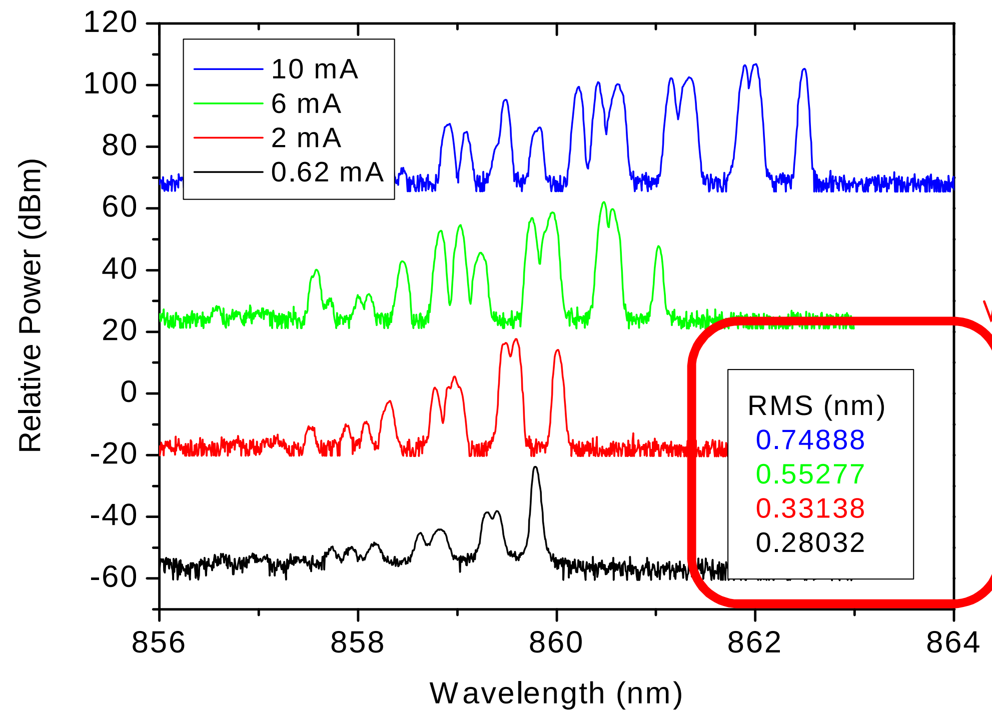
"conventional wisdom" = larger oxide apertures, larger *I* & *L*, relatively low *J*

$$f_r = D \cdot \sqrt{I - I_{th}}$$

$\uparrow I \rightarrow \uparrow \Delta\lambda_{RMS}$

Standard	allowed spectral width
10G Ethernet	0.45 nm
16G Fibre Channel	0.59 nm
40G & 100G Ethernet	0.65 nm





A. Mutig, Ph.D. dissertation, TUB, Berlin, Federal Republic of Germany (2011).

How can we achieve low fJ/bit operation?

Wavelength:

- 850, 980,1060,1250 nm?
  → trade offs, standards, application dependent requirements

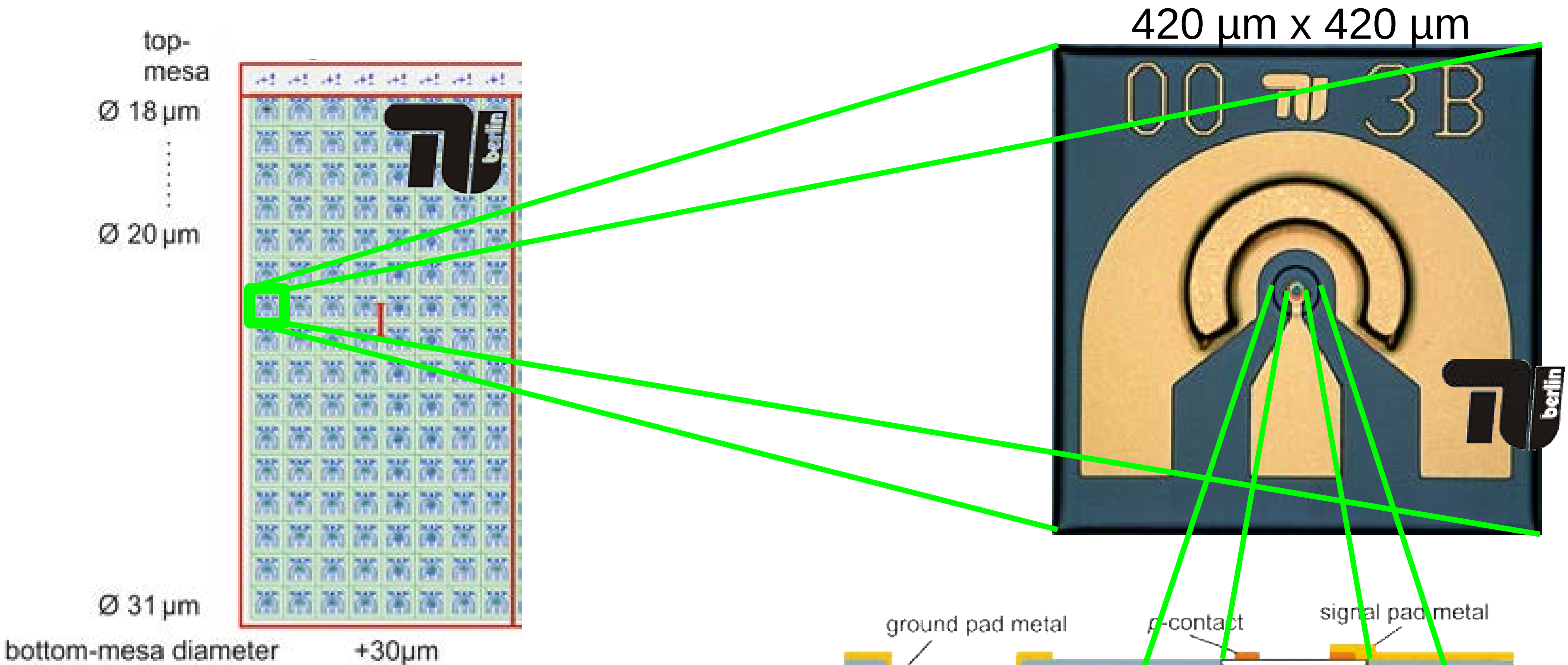
Strategy:

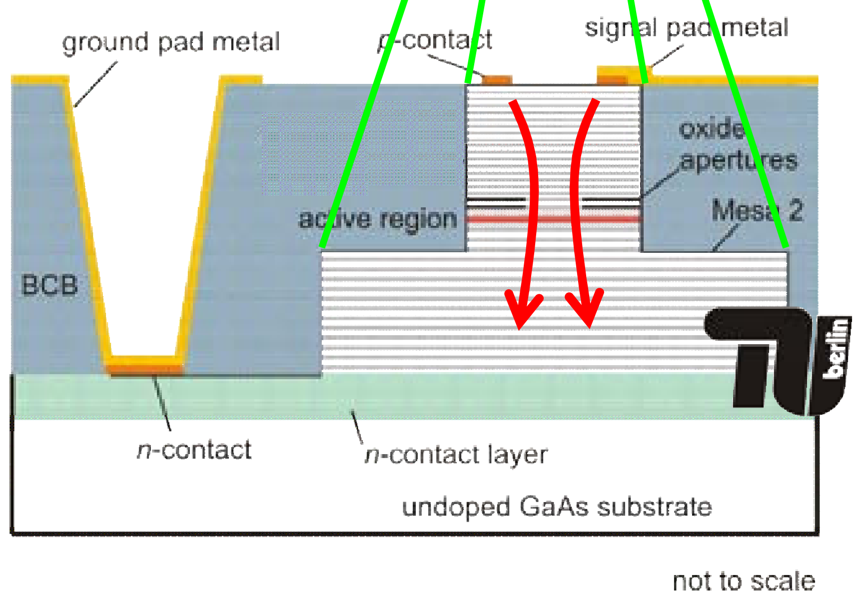
- use VCSELs with small (2-5 µm) oxide aperture diameter
  → benefit from high D-factor and low threshold electrical power
- operate VCSEL at low bias current
  → avoid self heating, low electrical power consumption
- decrease differential resistance to avoid self heating

Is this strategy compatible with:

- high bit rate operation?
- low current density operation?
- operation at high external temperatures?

VCSELs

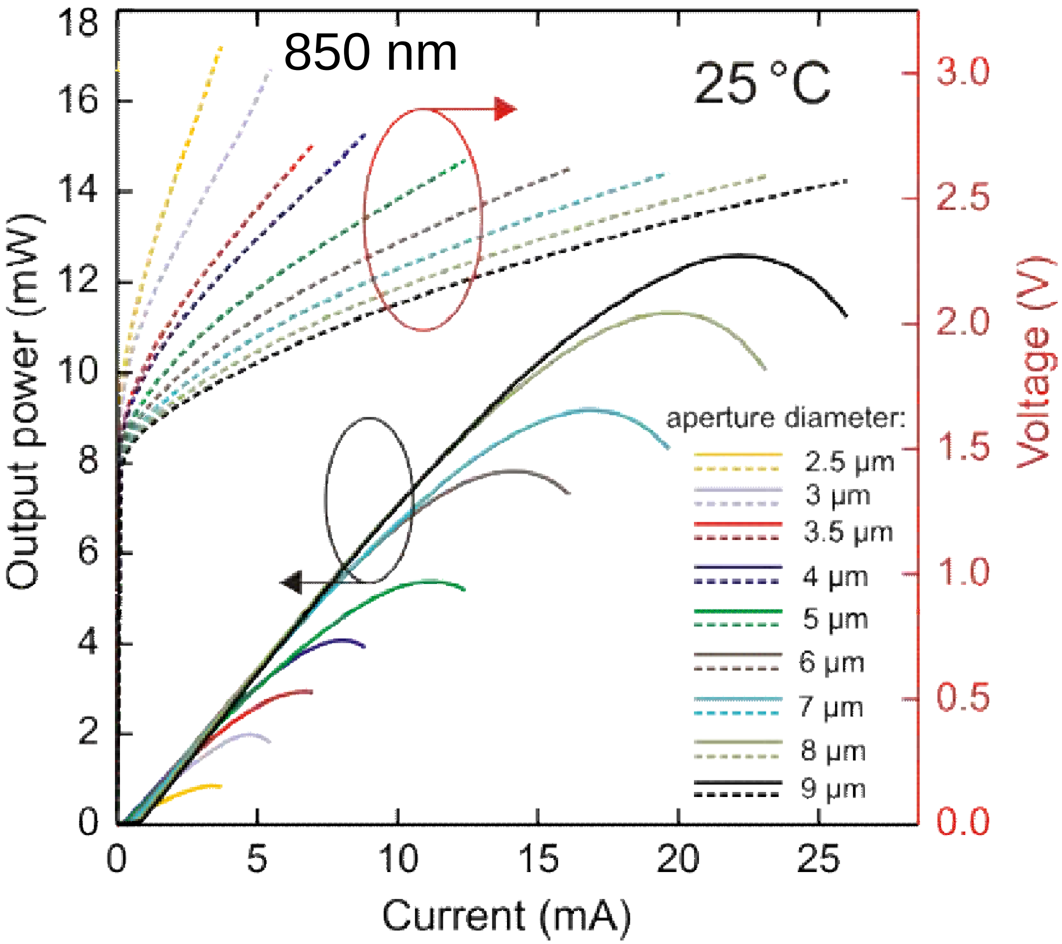


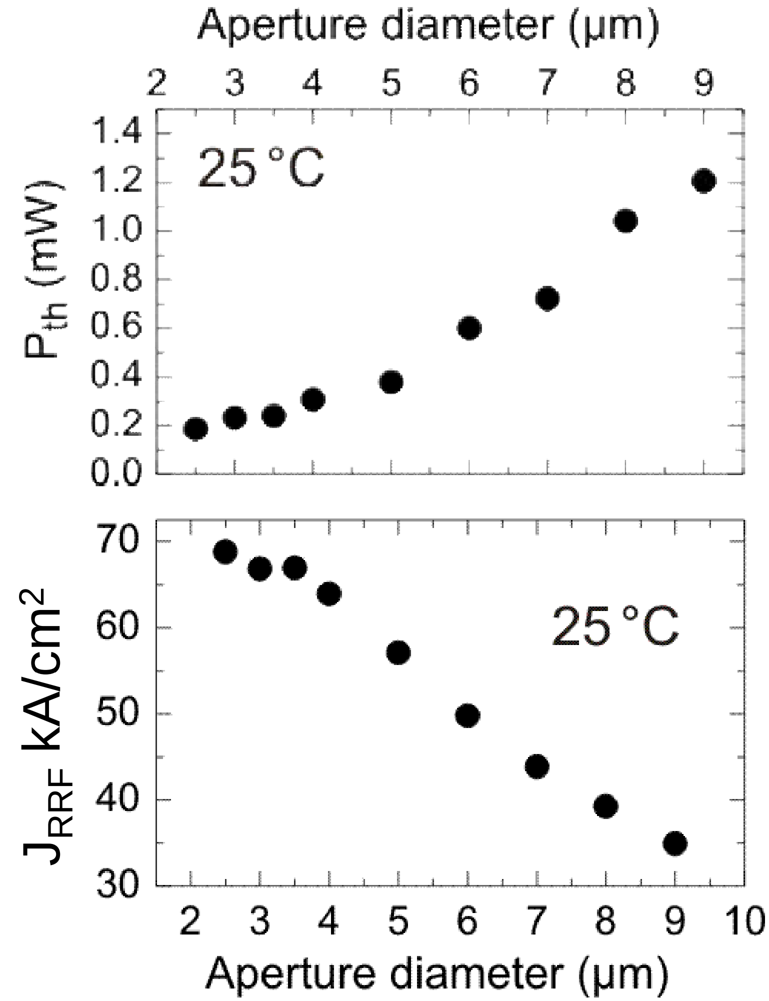


top mesa diameter: 18 to 31 µm
bottom mesa diameter: 48 to 61 µm

a group of 16 different oxide aperture diameter VCSELs in each column

CW characteristics





- 9 different oxide aperture diameters
- single-mode and multimode devices

P. Moser, …, D. Bimberg, IEEE JSTQE, 19 (4), 2013.